Amendments to the Specification:

1) page 1, first paragraph, please replace this paragraph with the following amended text:

The invention relates to the fabrication of integrated circuit devices, and more particularly, to a method for determining dielectric film properties. The method of the invention uses computer modeling of dielectric film properties whereby chemical bonding measurements are the input data that [[is]] are provided to the computer model.

2) page 4, last paragraph, page 5, first paragraph, please replace this paragraph with the following amended text:

Dielectric materials are frequently used for the creation of conductive interconnect lines, via or contact openings. In the formation of semiconductor integrated circuits, it is common practice to form interconnect metal line structures on a number of different levels within the structure and interconnecting the various levels of wiring with contact or via openings.

The first or lowest level of interconnect wires is typically formed in a layer of dielectric as a first step in the process after which a second or overlying level of interconnect wires is created in an overlying layer of dielectric over the first level.

The first level of interconnect wires is typically in contact with active regions in a semiconductor substrate but is not limited to such contact. The first level of interconnect can for instance also be in contact with a conductor that leads to other devices that form part of a larger, multi-chip structure.

The two levels of metal wires are connected by openings between the two ~~layers~~ levels, these openings [[that]] are created in [[the]] layers of surrounding dielectric and [[that]] are filled with metal where the openings ~~between the two layers are lines up with and match~~ align with contact points in one or both of the levels of metal lines.

3) page 6, last paragraph, page 7, page 8, first paragraph, please replace this paragraph with the following amended text:

This process of line formation in overlying layers [[on]] of metal can be repeated in essentially the same manner as [[just]] highlighted above for the first layer of interconnecting wires.

This process of forming sequential layers of interconnecting levels of wire is in many instances prone to problems and limitations. Copper has in recent times found more application in the use of metal wires due to its low resistivity, high electromigration resistance and stress voiding resistance.

Copper however exhibits the disadvantage of high diffusivity in common insulating materials such as silicon dioxide and oxygen-containing polymers. This leads to, for instance, the diffusion of copper into polyimide during high temperature processing of the polyimide resulting in severe erosion of the copper and the polyimide due to the copper combining with oxygen in the polyimide. The erosion may result in loss of adhesion, delamination, voids, and ultimately a catastrophic failure of the component.

The copper that is used in an interconnect may diffuse into the silicon dioxide layer, causing the dielectric ~~strength~~ to become conductive and also decreasing the dielectric strength of the silicon dioxide layer.

A copper diffusion barrier is therefore often required; silicon nitride is often applied as a diffusion barrier to copper. Silicon nitride however has a dielectric constant that is high compared [[to]] with silicon dioxide, thereby limiting the use of silicon nitride in encapsulating copper interconnect lines.

To further enhance the adhesion of a copper interconnect line to [[the]] a surrounding layer of dielectric or insulation, a seed layer is deposited over the barrier layer. A seed layer can be deposited using a sputter chamber or an Ion Metal Plasma (IMP) chamber at a temperature of between about 0 and 300 degrees [[C.]] C and a pressure of between about 1 and 100 mTorr, using copper or a copper alloy as the source at a flow rate of between about 10 and 400 sccm and using argon as an ambient gas. The minimum thickness of a seed layer is typically about 50 Angstrom, this thickness is required to achieve a reliable gap fill.

4) page 8, second paragraph, page 9, page 10, first paragraph, please remove the following text:

~~Scaling devices to smaller dimensions can lead to a multitude of undesirable effects. One of these effects is the increase in the capacitive coupling between conductors in the circuit. Therefore, it becomes impractical to reduce the RC time constant and cross talk between metal lines within today's multi-level metallization system.~~

~~The capacitance between conductors is highly dependent on the insulator or dielectric used to separate the lines. Conventional semiconductor fabrication commonly employs silicon dioxide as a dielectric that has a dielectric constant of about 3.9. The lowest possible, or ideal, dielectric constant is 1.0, which is the dielectric constant of a vacuum.~~

~~For a given interconnect layout, both power consumption and crosstalk decrease, and performance increases, as the dielectric constant of the insulator decreases. It has been found that using the same dielectric, scaling down from 0.50 um. to 0.25 um. will result in a 30% increase in power consumption. This power consumption can be decreased by more than 50% if SiO_2 is~~

~~replaced by oxide. This change is important for high frequency operation because power consumption increases proportionally with frequency.~~

~~Additionally, the crosstalk increases more than 50% when scaling down from 0.50 um. to 0.25 um. primarily due to the increase in line-to-line capacitance. The increase in the ration crosstalk/Vcc degrades the noise margin and circuit performance. Replacing SiO_2 with air will significantly reduce crosstalk because of the small dielectric constant of air, which is generally less than 1.001.~~

~~In the field of high density interconnect technology, many integrated circuit chips are physically and electrically connected to a single substrate commonly referred to as a multi-chip module (MCM). To achieve a high wiring and packing density, it is necessary to fabricate a multilayer structure on the substrate to connect integrated circuits to one another. Typically, metal power and ground planes in the substrate are separated by layers of a dielectric such as a polyimide. Embedded in other dielectric layers are metal conductor lines within the range of about 8 to 25p wide) with vias (holes) providing electrical connections between signal lines or to the metal power and ground planes. Adjacent layers are ordinarily~~

~~formed so that the primary signal propagation directions are orthogonal to each other. Since the conductor features are typically narrow in width and thick in a vertical direction (in the range of 5 to 10 microns thick) and must be patterned with microlithography, it is important to produce patterned layers that are substantially flat and smooth (i.e. planar) to serve as the base for the next layer.~~

5) page 18, first paragraph, please replace this paragraph with the following amended text:

Fig. 2 shows a set of graphic presentations of the effects of CVD chemical bonding on the flat band voltage V_{fb} of various dielectric materials. The values and materials that are plotted along the X axis of Fig. 2 are identical to those of Fig. 1, the Y axis of Fig. 2 represents the flat band voltage V_{fb} of the dielectric.

Observations can be made relative to the graphs that are shown in Fig. 2 that are similar to the previously made observations with respect to Fig. 1. It is of interest to note that, for most of the dielectric materials that are represented in Figs. 1 and 2, the slopes of the curves of Fig. 1 and Fig. 2 for a given material [[is]] <u>are</u> the same. This means that a

dielectric material that shows for instance an increase in the value of k with chemical bonding intensity [[ue]] shows a corresponding increase in the value of V_{fb}. This is however not universally true, a fact that will become apparent by comparing sections c, h and j of Fig. 1 with like-named sections in Fig. 2. ~~Where,~~ This comparison shows that, for instance, in section c of Fig. 1, the k value increases with increased chemical bonding, while the V_{fb} value (as shown in Fig. 2, section c) ~~increases~~ decreases. The same is true for ~~sections~~ graphic presentations h and j, [[(]]representing different dielectric materials[[)]], ~~h and j~~ of respectively Figs. 1 and 2.

6) page 20, second paragraph, please replace this paragraph with the following amended text:

Fig. 5 shows the effects of chemical bonding on the dielectric constant k of carbon doped SiO_2 dielectric material.

Fig. 5 shows, similar to Fig. 1, a set of graphic presentations of the effects of CVD chemical bonding on the dielectric constant k of various carbon doped SiO_2 dielectric materials.

The horizontal or X axis of the graph that is shown in Fig. 5 is subdivided [[in]] into various carbon doped SiO_2 dielectric materials, where for each of these materials is shown the effect that modified chemical bonding has on the dielectric constant.

The vertical or Y axis of the graph represents the dielectric constant k of the various carbon doped SiO_2 dielectric materials. The chemical bonding for each carbon doped SiO_2 material is measure by FTIR. The list of materials and wavenumbers is as follows: